

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Albert S. Weiner

Examiner: Nguyen, Thinh

Patent No.: 7,777,281

Group Art Unit: 2818

Issue Date: August 17, 2010

Docket No: 2800.450US1

Title: Non-volatile transistor memory array incorporating read-only elements with single mask set

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

ATTN: CERTIFICATE OF CORRECTION BRANCH

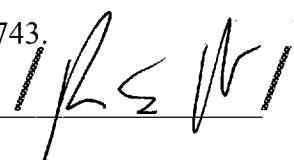
We are transmitting herewith the attached:

- ☒ Authorization to charge Deposit Account No. 19-0743 in the amount of \$100.00 to cover the Certificate of Correction Fee.
- ☒ Request for Certificate of Correction. (1 pg.)
- ☒ Certificate of Correction Form - PTO-1050 (1 pg.)

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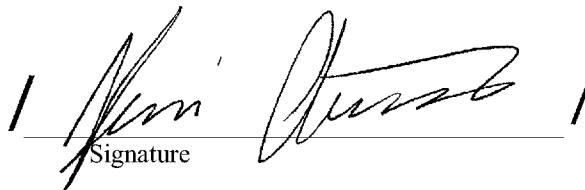
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 30 day of September, 2010.

Kevin Austad
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